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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/677,061	09/29/2000	James J. Delmonico	1	1686

22046 7590 06/20/2003

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EXAMINER	
LEE, CHRISTOPHER E	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 06/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/677,061	DELMONICO, JAMES J.	
	Examiner	Art Unit	
	Christopher E. Lee	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

In the claim 6, it recites the limitation "said bridge device returns a layered protocol message to said host bus master that includes a message field having data for a write command or a read count field for a read command". However, the disclosure fails to provide proper antecedent basis for the claimed limitation in the claims.

In the claims 9 and 24, they recite the limitation "an I^2C address for said target devices is represented in said CRC value", respectively. However, the disclosure fails to provide proper antecedent basis for the claimed limitation in the claims.

In the claim 28, it recites the limitation "at least two bridge devices coupled to said parent bus, said host bus master operable to use pairs of said bridge devices to verify data received from said target devices". However, the disclosure fails to provide proper antecedent basis for the claimed limitation in the claims.

Drawings

3. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

4. The drawings are objected to because the Figure 2, "Partner reset-in" doesn't have a reference sign "48", which is used in the disclosure, page 6, lines 21-23. However, the sign "48" is used for the "Event watchdog timer" in the drawing. Thus, the Examiner recommends (1) assigning a new reference

sign for the "Partner reset in" in Figure 2, and (2) correcting the text disclosure, page 6, lines 21-23, using the new assigned reference sign for the subject matter "Partner reset-in". A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

a. On page 8, lines 2-3, and 16, the reference sign 110 for LIP bridge is not shown in the drawings.

b. On page 9, line 15, the reference sign 120 for a four byte format is not shown in the drawings.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

6. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: In Figure 3, the reference sign "120" is not mentioned in the text disclosure. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

7. The drawings are objected to under 37 CFR 1.83(a) because they fail to show at least one host bus master including a digital processor as described in the specification, claim 27. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

8. Claims 1-25 and 27 are objected to because of the following informalities:

In lines 2-3 of the claim 1, substitute "said device comprising" by --said bridge device comprising" in order to clearly point out its appropriate subject matter.

In the claims 2-25 and 17-25, substitute "the device" in line 1 of each one of the claims, respectively, by --the bridge device-- for the same reason of above mentioned.

In the claims 2 and 4-8, substitute "said layered protocol" respectively, by --said layered communication protocol--.

In the claim 12, substitute "bust" in line 2, by --bus--.

In the claims 16, 18, 19 and 27, substitute "said second protocol" respectively, by --said second communications protocol--.

In the claims 16, 19 and 27, substitute "said first protocol" by --said first communications protocol--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

10. Claim 6 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In the claim 6, it recites the limitation "said bridge device returns a layered protocol message to said host bus master that includes a message field having data for a write command or a read count field for a read

command", which contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the Application was filed, had possession of the claimed invention. Instead, the Applicant discloses "a master write command (i.e., sending a layered protocol message) from the host bus master (i.e., host bus master) to the LIP bridge (i.e., bridge device) has a four byte format comprising LIP address+W, Child Address+R/W or Function, Data for Write (i.e., a message field having data for a write command) or Read Count and CRC (i.e., a read count field for a read command)" in lines 14-18 on page 9 and in Fig. 4 of the Application. Thus, the claim 6 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

11. Claims 9 and 24 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for calculating a CRC value being represented by a linear shift register with feedback taps given by the polynomial $X^8+X^5+X^4+1$, does not reasonably provide enablement for representing an I^2C address for target devices in said CRC value. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make/use the invention commensurate in scope with these claims. The Application states that a CRC code is a unique number that is related to the data in mathematical way such that in the data will result in a different CRC code (Application, page 5, lines 15-17). However, the Application is silent that an I^2C address for target devices is represented in said CRC code (i.e., CRC value). Furthermore, the Examiner doubts how to represent I^2C address for target devices in said CRC value in light of the specification.

12. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

13. Claims 1, 15, 17 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In the claims 1 and 26, they respectively recite the limitation "the number of addressable devices" in line 1. There is insufficient antecedent basis for this limitation in the claim. Thus, the term "the number of addressable devices" could be considered as --a number of addressable devices-- since it is not clearly defined in the claims.

In the claim 15, it recites the limitation "said bus" in line 1. There is insufficient antecedent basis for this limitation in the claim. Thus, the term "said bus" could be considered as --said child bus-- since it is not clearly defined in the claims.

In the claim 17, it recites the limitation "said layered protocol" in line 2. There is insufficient antecedent basis for this limitation in the claim. Thus, the term "said layered protocol" could be considered as --said first communications protocol-- since it is not clearly defined in the claims.

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

14. Claims 1-5, 13-18, 22, 23, 26 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Barenys et al. [US 6,145,036 A; hereinafter Barenys].

Referring to claim 1, Barenys discloses a bridge device (i.e., Expansion Processor 202 of Fig. 2) for expanding a number of addressable devices (i.e., a plurality of expansion devices) that can be connected to a communications bus (i.e., Primary Bus 203 of Fig. 2; See col. 3, lines 31-39), said devices using a predetermined protocol (i.e., said plurality of expansion devices using I^2C protocol; See col. 3, lines 22-29), said bridge device comprising: at least one parent bus port for coupling at least one host bus master (i.e., bus master on primary bus) over a parent bus (i.e., a primary bus; in fact, a port of said expansion processor for coupling a primary bus to said expansion processor in Fig. 2), said bus master operable to utilize a layered communication protocol (i.e., extended I^2C protocol for the communication

between primary bus master and sub-bus slave via expansion processor, such that Primary Bus Transfer Sequence 301 of Fig. 3A and 3B; See col. 5, line 60 through col. 7, line 17; in fact, the transaction sequence 300 includes primary bus transfer sequence 301 and sub-bus transfer sequence 302 in of Fig. 3A and 3B, wherein said expansion processor is an I^2C device implementing a communication protocol for said sub-bus transaction, layered on top of a standard I^2C protocol) having bridge device addressing capabilities (i.e., data bye 304 for expansion processor addressing in Fig. 3A; See col. 6, lines 7-9) and addressing characteristics of said predetermined protocol included therein (i.e., I^2C addressing characteristics; See col. 4, lines 18-22); at least one child bus port (i.e., a plurality of ports of said expansion processor for coupling sub-busses 1,2,... n to said expansion processor in Fig. 2) for coupling to target devices (e.g., expansion devices 215, 216 and 218 in Fig. 2) over a child bus (e.g., sub-bus 232 of Fig. 2), said target devices adapted to communicate using said predetermined protocol (See col. 5, lines 8-26); a digital processor (e.g., a conventional microcontroller having I^2C compatibility such as 83C751 or 87C751; See col. 3, lines 15-18) coupled to said parent bus port and said child bus port (i.e., in fact, said conventional microcontroller within said expansion processor, coupled to said primary bus and said sub-busses as shown in Fig. 2 implies that a digital processor coupled to said parent bus port and said child bus port), said digital processor operable to implement a protocol translator (See col. 5, lines 60+), said protocol translator operable to translate messages in said layered communication protocol on said parent bus port to said predetermined protocol output at said child bus port (See col. 6, lines 1-40; in fact, sub-bus code 307 and target device address 309 in layered communication protocol (i.e., extended I^2C protocol) translated to predetermined protocol (i.e., standard I^2C protocol) in Fig. 3 implies said protocol translator operable to translate messages (i.e., message of expansion device addressing bytes) in said layered communication protocol on said parent bus port to said predetermined protocol output at said child bus port) and to translate messages received at said child bus port in said predetermined protocol to said layered communication protocol to be output from said child bus port (See col. 6 line 41 through col.

7, line 17; in fact, read data bytes 329 and 334 in predetermined protocol (i.e., standard I^2C protocol) are echoed by expansion processor in layered communication protocol (i.e., extended I^2C protocol) in Fig. 3 implies said protocol translator operable to translate messages (i.e., message of expansion device data bytes) received at said child bus port in said predetermined protocol to said layered communication protocol (i.e., protocol of primary bus) to be output from said child bus port).

Referring to claims 2 and 17, Barenys respectively teaches said protocol translator is operable to pass through a message in said layered communication protocol onto said child bus to another bridge device coupled to said child bus (See col. 3, lines 30-33; i.e., wherein in fact that any one or more expansion devices may be another expansion processor coupled by one or more sub-buses to one or more expansion devices implies that said protocol translator is operable to pass through a message in said layered communication protocol onto said child bus (i.e., a message from a host bus master over a parent bus onto a child bus) to another bridge device coupled to said child bus (i.e., another expansion processor coupled by one or more sub-buses)).

Referring to claims 3 and 18, Barenys teaches said predetermined protocol is an I^2C protocol (See col. 3, lines 22-29), respectively.

Referring to claim 4, Barenys teaches a message (i.e., message from master on primary bus in Fig. 3) to said bridge device (i.e., expansion processor 202 of Fig. 2) in said layered communication protocol (i.e., extended I^2C protocol) includes a bridge address field (i.e., expansion processor address field 304 of Fig. 3A) and a target device address field (i.e., sub-bus code 307 and expansion device address 309 in Fig. 2, as combined).

Referring to claim 5, Barenys teaches said layered communication protocol (See Fig. 3) includes a read/write function indication (e.g., Read/Write 305 and 322 in Fig. 3) to said target devices (See col. 6, lines 10-12 and lines 41-45).

Referring to claim 15, Barenys teaches said child bus (e.g., sub-bus 232 of Fig. 2) is a two-wire bus (See col. 4, line 9).

Referring to claim 16, Barenys discloses a bridge device (i.e., Expansion Processor 202 of Fig. 2) for interfacing between a host bus master (i.e., bus master on primary bus 203 of Fig. 2; See col. 3, lines 31-39) and target devices (i.e., a plurality of expansion devices using I^2C protocol; See col. 3, lines 22-29) coupling to a two-wire electrical bus (i.e., sub-bus 232 of Fig. 2; See col. 4, line 9), said device comprising: a first transceiver coupled to said host bus master (i.e., communication means of bus master on primary bus) over a parent bus (i.e., a primary bus; in fact, a first transceiver coupled to said host bus master for I^2C transaction; See col. 3, lines 22-29), said host bus master utilizing a first communications protocol (i.e., extended I^2C protocol for the communication between primary bus master and sub-bus slave via expansion processor, such that Primary Bus Transfer Sequence 301 of Fig. 3A and 3B; See col. 5, line 60 through col. 7, line 17); a second transceiver coupled to said target devices (i.e., communication means of said expansion devices on sub-bus) over a child bus (i.e., sub-bus 232 of Fig. 2), said target devices utilizing a second communications protocol (i.e., a standard I^2C protocol; See col. 5, lines 8-26), said first communications protocol having a bridge device address field (i.e., expansion processor address field 304 of Fig. 3A) for addressing said bridge devices (See col. 6, lines 7-9) and a target device address field (i.e., sub-bus code 307 and expansion device address 309 in Fig. 2, as combined) for addressing said target devices coupled to said child bus (See col. 6, lines 22-27), where the number of target devices addressable by said host bus master is expandable based on the number of bridge device coupled thereto (See Abstract, col. 3, lines 30-33, and col. 4, lines 18-22); and a protocol translator (See col. 5, lines 60+) coupled to said first and second transceiver for translating communications in said first communications protocol destined for said target devices to said first communications protocol (See col. 6, lines 1-40; in fact, sub-bus code 307 and target device address 309 in extended I^2C protocol translated to standard I^2C protocol in Fig. 3 implies said protocol translator

coupled to said first and second transceiver for translating communications in said first communications protocol destined for said target devices to said first communications protocol) and translating communications in said first communications protocol destined for said bus master to said first communications protocol (See col. 6 line 41 through col. 7, line 17; in fact, read data bytes 329 and 334 in standard I^2C protocol are echoed by expansion processor in extended I^2C protocol in Fig. 3 implies said protocol translator translates communications in said first communications protocol destined for said bus master to said first communications protocol).

Referring to claims 13 and 22, Barenys teaches said bridge device (i.e., expansion processor 202 of Fig. 2) is a slave to said host bus master and a master of said child bus, respectively.

Referring to claims 14 and 23, Barenys respectively teaches said bridge device (i.e., expansion processor 202 of Fig. 2) provides isolation between said parent bus and said child bus (See col. 3, line 57 through col. 4, line 3; i.e., wherein in fact that if a DIMM fails, then only its particular sub-bus will fail, no failure in the primary bus implies that said bridge device provides isolation between said parent bus and said child bus).

Referring to claim 26, Barenys discloses a method for expanding a number of addressable devices (i.e., a plurality of expansion devices) which use a given protocol (i.e., a standard I^2C protocol; See col. 5, lines 8-26) that can be connected to a communications bus (i.e., Primary Bus 203 of Fig. 2; See col. 3, lines 31-39), said method comprising: providing a bridge device (i.e., Expansion Processor 202 of Fig. 2) having at least one parent bus port (i.e., a port of said expansion processor for coupling a primary bus to said expansion processor in Fig. 2) and at least one child bus port (i.e., a plurality of ports of said expansion processor for coupling sub-busses 1,2,... n to said expansion processor in Fig. 2) adapted for coupling, respectively, to a parent bus (i.e., coupling to primary bus) and a child bus (i.e., coupling to sub-bus); coupling to at least one host bus master to said parent bus (i.e., bus master over a primary bus), said bus master operable to utilize a layered communication protocol (i.e., extended I^2C protocol for the

communication between primary bus master and sub-bus slave via expansion processor, such that Primary Bus Transfer Sequence 301 of Fig. 3A and 3B; See col. 5, line 60 through col. 7, line 17; in fact, the transaction sequence 300 includes primary bus transfer sequence 301 and sub-bus transfer sequence 302 in of Fig. 3A and 3B, wherein said expansion processor is an I^2C device implementing a communication protocol for said sub-bus transaction, layered on top of a standard I^2C protocol) having bridge device addressing capabilities (i.e., data bye 304 for expansion processor addressing in Fig. 3A; See col. 6, lines 7-9) and addressing characteristics of said given protocol included therein (i.e., I^2C addressing characteristics; See col. 4, lines 18-22); coupling to said child bus target devices (e.g., expansion devices 215, 216 and 218 in Fig. 2) assigned to said bridge device (i.e., expansion processor in Fig. 2) and adapted to communicate using said given protocol (See col. 5, lines 8-26); translating messages in said layered communication protocol received on said parent bus port to said given protocol to be output at said child bus port (See col. 6, lines 1-40; in fact, sub-bus code 307 and target device address 309 in layered communication protocol (i.e., extended I^2C protocol) translated to predetermined protocol (i.e., standard I^2C protocol) in Fig. 3 implies translating messages in said layered communication protocol received on said parent bus port to said given protocol to be output at said child bus port) and translating messages received at said child bus port in said given protocol to said layered communication protocol to be output from said child bus port (See col. 6 line 41 through col. 7, line 17; in fact, read data bytes 329 and 334 in predetermined protocol (i.e., standard I^2C protocol) are echoed by expansion processor in layered communication protocol (i.e., extended I^2C protocol) in Fig. 3 implies translating messages received at said child bus port in said given protocol to said layered communication protocol to be output from said child bus port). Refer to col. 5, lines 60+.

Referring to claim 27, Barenys discloses a system (i.e., I^2C expansion apparatus 200 of Fig. 2) comprising: at least one host bus master (i.e., bus master over a primary bus) including a digital processor (i.e., means for transmitting/receiving data on primary bus using extended I^2C protocol), said host bus

master operable to utilize a first communications protocol (i.e., extended I^2C protocol for the communication between primary bus master and sub-bus slave via expansion processor, such that Primary Bus Transfer Sequence 301 of Fig. 3A and 3B; See col. 5, line 60 through col. 7, line 17) for communicating over a parent bus (i.e., primary bus 203 of Fig. 2); and at least one bridge device (i.e., Expansion Processor 202 of Fig. 2) including, a first transceiver coupled to said host bus master (i.e., communication means of bus master on primary bus) over said parent bus (i.e., a primary bus; in fact, a first transceiver coupled to said host bus master for I^2C transaction; See col. 3, lines 22-29), said host bus master utilizing a first communications protocol (i.e., extended I^2C protocol for the communication between primary bus master and sub-bus slave via expansion processor, such that Primary Bus Transfer Sequence 301 of Fig. 3A and 3B; See col. 5, line 60 through col. 7, line 17); a second transceiver coupled to target devices (i.e., communication means of said expansion devices on sub-bus) over a child bus (i.e., sub-bus 232 of Fig. 2), said target devices utilizing a second communications protocol (i.e., a standard I^2C protocol; See col. 5, lines 8-26), said first communications protocol having a bridge device address field (i.e., expansion processor address field 304 of Fig. 3A) for addressing said bridge devices (See col. 6, lines 7-9) and a target device address field (i.e., sub-bus code 307 and expansion device address 309 in Fig. 2, as combined) for addressing said target devices coupled to said child bus (See col. 6, lines 22-27); and a protocol translator (See col. 5, lines 60+) coupled to said first and second transceiver for translating communications in said first communications protocol destined for said target devices to said first communications protocol (See col. 6, lines 1-40; in fact, sub-bus code 307 and target device address 309 in extended I^2C protocol translated to standard I^2C protocol in Fig. 3 implies said protocol translator coupled to said first and second transceiver for translating communications in said first communications protocol destined for said target devices to said first communications protocol) and translating communications in said first communications protocol destined for said bus master to said first communications protocol (See col. 6 line 41 through col. 7, line 17; in fact, read data bytes 329 and 334

in standard I^2C protocol are echoed by expansion processor in extended I^2C protocol in Fig. 3 implies said protocol translator translates communications in said first communications protocol destined for said bus master to said first communications protocol).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 7 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barenys [US 6,145,036 A] in view of Willems [US 5,613,090 A].

Referring to claims 7 and 19, Barenys discloses all the limitations of the claims 7 and 19, respectively, except that does not teach said protocol translator includes a packet parser and dispatch mechanism for separating packets in said layered communication protocol and dispatching packets of said predetermined protocol over child bus.

Willems discloses a computer system (i.e., server in Fig. 1), wherein a protocol translator (i.e., translation layer 12 of Fig. 1) includes a packet parser and dispatch mechanism (i.e., parser/dispatcher layer 30 of Fig. 2) for separating packets (i.e., breaking down packets) in a layered communication protocol (i.e., X protocol) and dispatching packets of a predetermined protocol (i.e., CPQ protocol; See col. 3, line 35) over child bus (i.e., communication interface between UNIX machine 11 and Windows machine 13 in Fig. 1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said packet parser/dispatcher, as disclosed by Willems, in said protocol translator, as disclosed by Barenys, for the advantage of providing said bridge device (i.e., server) a capability of providing nearly seamless integration of said addressable devices (i.e., "X WINDOWS" applications) into

said host bus master (i.e., "MICROSOFT WINDOWS" environment; See Willems, col. 1, line 66 through col. 2, line 2).

17. Claims 8 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barenys [US 6,145,036 A] in view of Szczepanek [US 6,414,956 B1].

Referring to claims 8 and 20, Barenys discloses all the limitations of the claims 8 and 20, respectively, except that does not teach a standard format message in said layered communication protocol includes a CRC field having a value based on other data included in said message, said device further including CRC generator and checker.

Szczepanek discloses a VLAN tag transport within a switching device 400 (Fig. 4), wherein a standard format message (i.e., tagged Ethernet frame in Fig. 1) in a layered communication protocol (e.g., TCP/IP; See col. 1, lines 15-20) includes a CRC field (i.e., FCS (32-bit CRC) 124 of Fig. 1) having a value based on other data included in said message (See col. 3, lines 45-51; i.e., wherein in fact that a frame check sequence (FCS) value based on the content of the packet implies that a CRC field has a value based on other data included in said message); CRC generator (i.e., means for computing said FCS (32-bit CRC); See col. 3, lines 47-50) and checker (i.e., means for comparing said FCS (32-bit CRC) with a calculated CRC of received packet; See col. 3, lines 50-53).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said error detection mechanism using CRC (Cyclic Redundancy Check), as disclosed by Szczepanek, in said bridge device, as disclosed by Barenys, for the advantage of providing error detection in the case where line errors or transmission collisions in said communication bus (i.e., Ethernet) result in corruption of said standard format message (i.e., MAC frame; See Szczepanek, col. 1, line 66 through col. 2, line 2).

18. Claims 10 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barenys [US 6,145,036 A] in view of Szczepanek [US 6,414,956 B1] as applied to claims 8 and 20 above, and further in view of Youn [US 6,219,691 B1].

Referring to claims 10 and 25, Barenys, as modified by Szczepanek, discloses all the limitations of the claims 10 and 25, respectively, including said bridge device (i.e., expansion processor; Barenys) returns said standard format message (i.e., tagged Ethernet frame in Fig. 1; Szczepanek) to a host bus master (i.e., returning data from expansion device to bus master on primary bus via expansion processor; Barenys) except that does not teach said host bus master can identify communications from a specific target device based on a tag field and a CRC value.

Youn discloses a communication circulation system 100 (Fig. 1), wherein a host bus master (i.e., communication circulation device 110 of Fig. 1) can identify communications (See col. 3,,lines 14-20) from a specific target device (i.e., a terminal, which launches a message with a tag code identifying an area of interest) based on a tag field (i.e., tag 606 of Fig. 9, which is for identifying said area of interest, viz., intended destination) and a CRC value (i.e., CRC for identifying (viz., verifying) message integrity; See col. 7, lines 37-38).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said target device identification feature based on said tag field, as disclosed by Youn, in said host bus master, as disclosed by Barenys, as modified by Szczepanek, for the advantage of providing a communication identifying system (i.e., communication circulation system) that receives a communication message (i.e., a first party message) that is addressed or destined to an area of interest of said communication message (See Youn, col. 1, lines 1-3).

19. Claims 11 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barenys [US 6,145,036 A] in view of Philips [The I^2C-Bus Specification, Version 2.1, published by Philips Semiconductors, January, 2000; cited by the Applicant on page 8, in lines 9-15 of the Application].

Referring to claims 11 and 21, Barenys discloses all the limitations of the claims 11 and 21, respectively, except that does not teach said parent bus is coupled to multiple host bus masters, and a command collision detector for determining whether said multiple host bus masters have commands pending on said parent bus.

Philips discloses an I^2C-Bus Specification (Version 2.1), wherein a parent bus (i.e., I^2C-Bus) could be coupled to multiple host bus masters (See page 6, Chapter 2.2; i.e., multi-master capability of the I^2C-Bus protocol), and a command collision detector (i.e., collision detection) for determining whether said multiple host bus masters (i.e., multi-masters) have commands pending on said parent bus (See page 4, Chapter 2; i.e., wherein in fact that it's a true multi-master bus including collision detection and arbitration to prevent data corruption if two or more masters simultaneously initiate data transfer implies that a command collision detector for determining whether said multiple host bus masters have commands pending on said parent bus).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said multi-master capability having collision detection, as disclosed by Philips, in said parent bus, as disclosed by Barenys, for the advantage of allowing rapid testing and alignment of end-user equipment via external connections to an assembly-line of equipment manufacturers (See Philips, page 6, Chapter 2.2).

20. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Barenys [US 6,145,036 A] in view of Kubo [US 5,586,269 A].

Referring to claim 12, Barenys discloses all the limitations of the claim 12 except that does not teach a special function command engine for receiving and processing special commands from said host bust master.

Kubo discloses a communication control device, wherein a special function command engine (i.e., control device 22 of Fig. 3) for receiving (i.e., home bus transmit/receive unit 23 of Fig. 3) and processing (i.e.,

processing unit 25 of Fig. 3) special commands (i.e., special command, referred to as "dummy command" in the reference) from a host bus master (i.e., from another control device, such as control device 2 in Fig. 1; See col. 4, lines 44-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said control device (i.e., special function command engine), as disclosed by Kubo, in said devices including bridge device, as disclosed by Barenys, for the advantage of providing a system for connecting said devices (i.e., communication control device) to said communication bus (i.e., home bus) of said I^2C communication system (i.e., information transmission system) in which the self-address of said device (i.e., control device) can be automatically set (See Kubo, col. 2, lines 57-60).

21. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Barenys [US 6,145,036 A] in view of Khosrowpour [US 6,202,115 B1].

Referring to claim 28, Barenys discloses all the limitations of the claim 28 except that does not teach at least two bridge devices coupled to said parent bus, said host bus master operable to use pairs of said bridge devices to verify data received from said target devices.

Khosrowpour discloses a fault tolerant redundant bus bridge systems, wherein at least two bridge devices (i.e., first bus bridge 110 and second bridge 120 in Fig. 1) coupled to a parent bus (i.e., first bus 101 of Fig. 1), a host bus master (e.g., host device) operable to use pairs of said bridge devices to verify data received from a target devices (e.g., RAID controllers; See col. 2, lines 35-41; i.e., wherein in fact that the first and second bus bridges may comprise respective first and second RAID controllers which are operative to communicate information from a host device connected to the first bus to a mass storage element connected to the second bus in a manner appropriate to implement one or more RAID levels implies that a host bus master operable to use pairs of said bridge devices to verify data (i.e., failover capability) received from a target devices (i.e., mass storage element)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said fault tolerant redundant bus bridge system, as disclosed by Khosrowpour, in said system, as disclosed by Barenys, for the advantage of providing improved performance, relaiability and data protection (See Khosrowpour, col. 2, lines 9-11).

Conclusion

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

With regard to I^2C Bus,

Son [US 6,233,635 B1] discloses diagnostic/control system using a multi-level I2C bus.

Faust et al. [US 6,205,504 B1] disclose externally provided control of an I^2C bus.

Stancil [US 5,897,663 A] discloses host I^2C controller for selectively executing current address reads to I^2C EEPROMS.

With regard to I^2C Protocol Packet,

Klein et al. [US 6,145,102 A] disclose transmission of an error message over a network by a computer which fails a self-test.

With regard to Multi-Protocol communication,

Marsanne et al. [US 5,884,044 A] disclose dedicated DDC integrable multimode communications cell.

Bellenger [US 5,949,786 A] discloses stochastic circuit identification in a multi-protocol network switch.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone numbers for the organization where this

application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Christopher E. Lee
Examiner
Art Unit 2189

cel/
June 14, 2003

RUPAL DHARIA
PRIMARY EXAMINER